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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,880	06/24/2003	Ian Robinson	NG(ST)-6447	8674

7590 05/27/2005

Christopher P. Harris
1111 Leader Building
526 Superior Avenue
Cleveland, OH 44114

EXAMINER	
HAROON, ADEEL	
ART UNIT	**PAPER NUMBER**
2685	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,880	ROBINSON ET AL.	
	Examiner	Art Unit	
	Adeel Haroon	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,11-18 and 20-28* is/are rejected.

7)☒ Claim(s) *7-10,13 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. Claims 1-16 and 18-28 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim1-29 of copending Application No. 10/606,093 in view of Budnik (U.S. 6,043,707). The only difference between the claims of the two applications is that the instant application claims has an added mode of envelope tracking. However, Budnik discloses a multi-mode amplifier with all three modes of linear, envelope mode, and polar that operates according to threshold values (Column 4, lines 44-54). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to add the mode of envelope tracking as taught by Budnik to the claimed system of Application No. 10/606,093 in order to encompass a commonly used mode in amplifiers thereby enhancing the features of the amplifier system.

This is a provisional obviousness-type double patenting rejection.

Specification

2. Claim 13 is objected to because of the following informalities: Claim 13 as written is dependent on claim 11 when it should be dependent from claim 12. It was assumed as such in the claim examination. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 6, 11-14, 20, 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Budnik (U.S. 6,043,707).

With respect to claim 1, Budnik discloses an amplifier system that operates on in three modes: envelope tracking mode, polar (envelope supply) mode, and linear mode based on characteristic of the input signal (Column 2, lines 58-67). Budnik in figure 8 discloses a power amplifier, element number 6 to amplify an input signal having an input terminal, element number 202, and a supply terminal, element number 207 (Column 6, lines 51-65). Budnik also discloses a mode selector/digital predistortion block, element number 1, controls the operation of the amplifier system and provides a selected amplifier input to the input terminal and selected amplifier supply signal to the supply terminal (Column 6, lines 35-42).

With respect to claim 2, Budnik discloses that the amplifier system operates in the linear mode for low level signals, the polar mode for highest level signals, and in the envelope tracking mode for signals in between the two levels (Column 2, lines 58-67).

With respect to claim 6, Budnik discloses a predistortion component, element number 1, that modifies the input and supply terminal digital domain to mitigate output distortion of the power amplifier (Column 8, lines 5-42).

With respect to claim 11, Budnik discloses a feedback path and digital predistortion block that compensate for variations in age and temperature of the amplifier system (Column 6, lines 5-30 and Column 5, lines 61-65).

With respect to claim 12 and 13, Budnik discloses that the amplifier system is to be used in wireless communication systems (Column 1, lines 8-11). Transmitters and base stations are basic components in a wireless communication system.

With respect to claim 14, Budnik discloses a delay, element number 37, that is used to delay the amplifier input and the supply signal (Column 6, lines 31-33). Budnik also discloses generating a supply signal with additional overhead, acceptable headroom, when operating in the envelope tracking mode (Column 7, lines 11-23).

With respect to claim 20, Budnik discloses an amplifier system the amplifying a phase and amplitude modulated input signal and means for switching modes of operation of the amplifier system between an envelope tracking mode, polar mode, and a linear mode base on an amplitude level of the input signal relative to a first threshold value and a second threshold value (Column 2, lines 58-67). Budnik also discloses the amplifier system operates in the linear mode for input signal amplitudes below about the first threshold value, 5 volts, the polar mode for input signal amplitudes above the second threshold level, 10 volts, and in the envelope tracking mode for input signal

amplitudes between the first and second threshold level, 5-10 volts (column 4, lines 44-52).

With respect to claim 23, Budnik discloses a predistortion component, element number 1, that modifies facilitates the amplifier system efficiency and mitigates out-of band emissions (Column 8, lines 5-42).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-4, 15-17, 21, 24, 25, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Budnik in view of Gailus et al. (U.S. 6,449,465).

With respect to claim 3, Budnik discloses providing a composite signal component, element number 490, to the input terminal and an amplitude modulation waveform, element number 498, which can be a constant envelope signal or a variable amplitude signal depending whether in linear mode or envelope tracking mode, to the supply terminal in figure 6 (Column 3, lines 50-65). Budnik does not specifically disclose the amplification technique in polar mode as recited in the claim. However, Gailus et al. discloses an amplification system in polar mode that teaches a DSP/mode selector, element number 401 providing an amplitude component, element number 402, of the input signal to the supply terminal and a phase component, element number 405,

of the input signal to the input terminal of a power amplifier, element number 410 (Column 5, line 63 – Column 6, line 11). Therefore, it would be obvious to one of ordinary skill in the art at the time of applicant's invention, to apply Gailus et al.'s polar mode amplifying technique to the multi mode amplifier system of Budnik to provide a specific amplifying method for the polar mode.

With respect to claim 4, Budnik does not disclose digital-to-analog converters. However, Gailus et al. discloses a digital-to-analog converter, element number 406, that converts the input and supply representations from the mode selector, element number 401, into analog signals and are coupled to the input and supply signal paths respectively (Column 5, lines 53-63). Gailus et al. also discloses a power supply/modulation amplifier, element number 426, in the supply path that modulates the amplitude of he supply signal (Column 6, lines 18-21). Therefore, it would be obvious to one of ordinary skill in the art at the time of applicant's invention, to apply Gailus et al.'s digital-to-analog conversion technique to the multi mode amplifier system of Budnik to convert the signals to analog so the signals are ready to be transmitted.

With respect to claim 15, Budnik in figure 8, discloses an amplifier system that comprises a power amplifier, element number 6 and a modulator/modulation amplifier, element number 43, having an output coupled to a supply terminal of the power amplifier. Budnik also discloses a digital system, circuit 800 except the power amplifier 6, that controls the operation of the amplifier system between an envelope tracking mode, polar mode, and a linear mode base on an amplitude level of the input signal relative to a first threshold value and a second threshold value (Column 2, lines 58-67).

Budnik also discloses the amplifier system operates in the linear mode for input signal amplitudes below about the first threshold value, 5 volts, the polar mode for input signal amplitudes above the second threshold level, 10 volts, and in the envelope tracking mode for input signal amplitudes between the first and second threshold level, 5-10 volts (column 4, lines 44-52). Budnik does not disclose the DACs as recited in the claim. However, Gailus et al. discloses a digital-to-analog converter, element number 406, that converts the input and supply representations from the digital system, element number 401, into analog signals and are coupled to the input and supply signal paths respectively (Column 5, lines 53-63). Therefore, it would be obvious to one of ordinary skill in the art at the time of applicant's invention, to apply Gailus et al.'s digital-to-analog conversion technique to the multi mode amplifier system of Budnik to convert the signals to analog so the signals are ready to be transmitted.

With respect to claims 16 and 21, Budnik discloses providing a composite signal component, element number 490, to the input terminal and an amplitude modulation waveform, element number 498, which can be a constant envelope signal or a variable amplitude signal depending whether in linear mode or envelope tracking mode, to the supply terminal in figure 6 (Column 3, lines 50-65). Budnik does not specifically disclose the amplification technique in polar mode as recited in the claim. However, Gailus et al. discloses an amplification system in polar mode that teaches a digital system, element number 401 providing an amplitude component, element number 402, of the input signal to the supply terminal and a phase component, element number 405, of the input signal to the input terminal of a power amplifier, element number 410

(Column 5, line 63 – Column 6, line 11). Therefore, it would be obvious to one of ordinary skill in the art at the time of applicant's invention, to apply Gailus et al.'s polar mode amplifying technique to the multi mode amplifier system of Budnik to provide a specific amplifying method for the polar mode.

With respect to claim 17, Budnik further discloses generating a supply signal with additional overhead, acceptable headroom, when operating in the envelope tracking mode (Column 7, lines 11-23).

With respect to claim 24 and 28, Budnik discloses a method for switching modes of operation of the amplifier system between an envelope tracking mode, polar mode, and a linear mode base on an amplitude level of the input signal relative to a first threshold value and a second threshold value corresponding to low and peak level amplitude signals (Column 2, lines 58-67). Budnik discloses providing a composite signal component, element number 490, to the input terminal and an amplitude modulation waveform, element number 498, which can be a constant envelope signal or a variable amplitude signal depending whether in linear mode or envelope tracking mode, to the supply terminal in figure 6 (Column 3, lines 50-65). Budnik further discloses generating a supply signal with additional overhead, acceptable headroom, when operating in the envelope tracking mode (Column 7, lines 11-23). Budnik does not specifically disclose the amplification technique in polar mode as recited in the claim. However, Gailus et al. discloses an amplification system in polar mode that teaches a digital system, element number 401 providing an amplitude component, element number 402, of the input signal to the supply terminal and a phase component,

element number 405, of the input signal to the input terminal of a power amplifier, element number 410 (Column 5, line 63 – Column 6, line 11). Therefore, it would be obvious to one of ordinary skill in the art at the time of applicant's invention, to apply Gailus et al.'s polar mode amplifying technique to the amplification method of Budnik to provide a specific amplifying method for the polar mode.

With respect to claim 25, Budnik discloses that the amplification method is to be used in wireless communication systems (Column 1, lines 8-11). Therefore, it would be used to transmit the amplified signal to at least one receiver.

With respect to claim 27, Budnik further discloses a predistortion component, element number 1, that modifies facilitates the amplifier system efficiency and mitigates out-of band emissions (Column 8, lines 5-42).

7. Claims 5, 18, 22, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Budnik and Gailus et al. further in view of Eidson et al. (U.S. 6,681,101).

The modified amplifier system of Budnik and Gailus et al. is described above in the discussion of claims 4, 16, 20 and 24. Even though Gailus et al. discloses a digital-to-analog converter, Gailus et al. does not specifically describe the DAC as a delta-sigma DAC. However, Eidson et al. discloses an amplifier system in a transmitter that teaches using a delta-sigma DAC that converts the digital components of the signal into the analog domain directly at a desired radio transmission frequency (Column 3, lines 56-61). Therefore, it would be obvious to one of ordinary skill in the art at the time of

the applicant's invention, to apply Eidson et al.'s teachings of using a delta-sigma DAC to the modified amplifier system of Budnik and Gailus et al. to convert the signal directly to the desired radio transmission frequency.

Allowable Subject Matter

8. Claims 7-10 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The specific digital cross cancellation technique as recited in the claims was not found nor fairly suggested in the prior art.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lindoff et al. (U.S. 6,101,224) discloses a polar modulation technique using a power amplifier. Midya et al. (U.S. 6,141,541) discloses an envelope modulation technique. Anzil (U.S. 6,236,237) discloses a linearization process for an amplifier system. Walker (U.S. 6,445,247) and Nilsson (U.S. 6,892,057) both disclose a self-controlled amplifier system based on threshold levels of the input signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adeel Haroon whose telephone number is (571) 272-

7405. The examiner can normally be reached on Monday thru Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AH
5/25/05

EDWARD F. URBAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600